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MODELLING AND DESIGNING OF CASCADED 9 LEVEL VOLTAGE SOURCE CONVERTER BASED ON DVR FOR MITIGATING HARMONICS IN DISTRIBUTED POWER SYSTEMUSING UNIT VECTOR

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ABSTRACT

The objective is to mitigate power quality problems and its occurrence on the distributed lines in power system field. Here, the harmonics are voltage sag, swell, total harmonic distortion and power factor correction. The capacitor supported dynamic voltage restorer (DVR) was designed with the 9 level cascaded multilevel inverter (MLI). This paper utilizes the error signal to control the triggering of the switches of an inverter using unit vector of space vector modulation and pulse width modulation inverter presage compensation scheme. SRFT has also been used for conversion of voltage from rotating vector to stationary. Main goal was to reduce power quality problems like sag, swell, and harmonics and power factor correction. Simulation results have been verified with and without MLI.

KEYWORDS: 9 Level Cascaded MLI, SVM PWM (Unit Vector) & DVR

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Original Article

INTRODUCTION

Power system fields are of two variants, such as transmission lines and distribution lines power system field. The consumers usually expect interrupted electricity supply without having any knowledge about the source or supply. Even the industrial and commercial bodies expect high load and uninterrupted power supply. When we focus on distributed lines, they mostly have nonlinear loads and critical loads. More number of harmonics occurs in the distribution line because of these loads. If one expects uninterrupted and high quality power supply, this means there should be zero harmonics in the distribution lines. Many flexible alternating current transmission system (FACTS) devices are available, such as C which is used to increase the transfer capacity in distribution network. FACTS are power electronics-based static devices. These are used to minimize the harmonics in distribution lines.

Voltage sag occurs if any faults is detected in the transmission lines or distribution lines, or if any large load changes are observed. If there is power line switching, and any additional loads are utilized by the consumers, then this leads to voltage swell. These harmonics are very harmful and can damaged as well as decrease the life span of loads. DVR is a custom powered device which is connected in between the source and load. It's main purpose is to compensate the harmonics like sag swell. Because of switching operations, consumers using washing machine and current heaters faced power fluctuations and flickering of lights. Hence, harmonics like sag, swell and

flickers are minimized by using power quality circuit in distribution lines.

By good quality, it means: low phase unbalance, less flickering in load voltage, less deformation in load voltage due to harmonics, level and extent of overvoltage and under voltage within specific limits and no power interruptions.

POWER QUALITY

The power quality circuit delivered quality power in transmission lines and distribution lines. This circuit is connected to distribution line in between source and load and is developed based on FACTS. In this paper, main purpose of power quality circuit is to mitigate harmonics in distribution lines.

Power Quality Problems

In power system field power quality is affected in many reasons. Power quality problems occur in power system networks. Hence, these networks produce non-standard voltage, thereby maintaining the quality power care in distribution lines FACTS. The power quality problems are sag, swell, flickers, etc. These harmonics are reduced by using FACTS in distribution lines.

DYNAMIC VOLTAGE RESTORER (DVR)

A DVR is custom power device, which is connected to the distribution lines in series. This device's main aim is that it injects the missing voltage in to the system for maintaining the load voltage to constant. Its location in the distribution lines is in between source supply and sensitive loads. DVR maintains continuous power quality and also quickly compensates the power quality problems like sag, swell, flickers, etc. There are different control techniques implemented in DVR. DVR operation principle involves injection of a voltage through an injection coupling transformer that is the difference between pre-sag and sagged voltage.

Figure 1 shows a block diagram of DVR consisting of 1) Injection Transformer 2)LC Filter 3) Voltage Source Converter or Inverter (VSC or VSI) and 4)Control System or Control unit and 5) Capacitor.

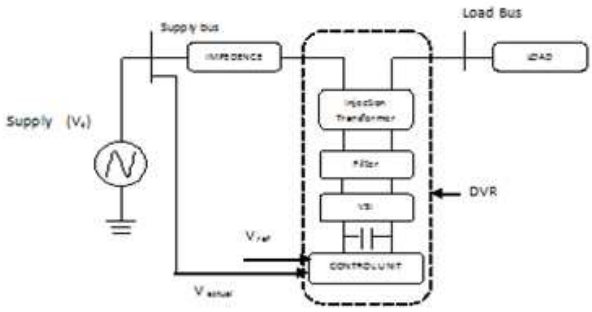

Figure 1: DVR Block Diagram

EQUIVALENT CIRCUIT OF DVR

Figure 2 shows equivalent circuit of DVR. It consists of source voltage V source, Source impedance Zs, Impedance of dvrZdvr and Injecting voltage Vinj.

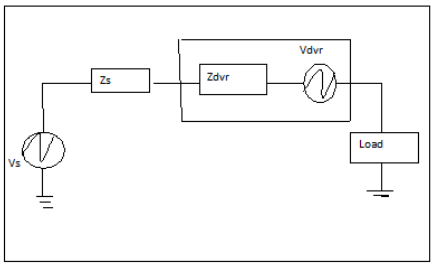

Figure 2: Equivalent Circuit of DVR

CASCADED NINE-LEVEL INVERTER

A single phase of this inverter consists of four simple H-bridge inverters, each can produce three output voltages +Vdc, 0 or –Vdc, thus the whole inverter can produce nine voltage levels. Each H-bridge will be switched on and off only once during each half cycle of the main harmonic. The harmonics produced by this way will be the main harmonic in addition to odd sine harmonics only. Figure 3 shows the structure of a single phase of this inverter. This multi-level inverter is made from several full-bridge inverters. The AC outputs for each different level of the full bridge inverters are connected in series so that the synthesized voltage waveform becomes the sum of the inverter outputs.

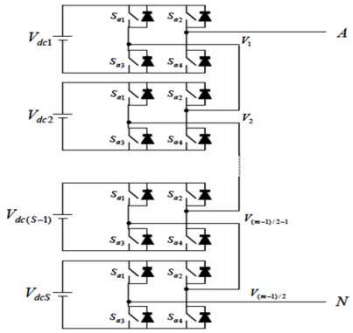

Figure 3: Power Electronic based Circuit of Nine Level Inverter

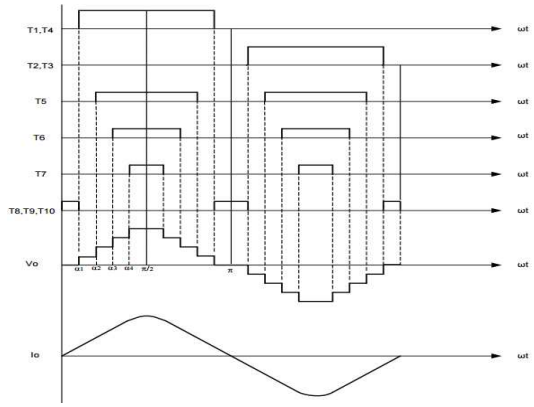

Figure 4: Switching Pulses of Nine Level Inverter

Control Scheme

The principle contemplations for the control of a DVR are identification of the starting and completion of the hang, voltage reference era, transient and unfaltering state control of the infused voltage and security of the system. Any

control technique implemented to control the DVR should fulfil all the above aspects. The basic idea behind the control strategy is to find the amount by which the supply voltage is dropped. For this, the three phase supply voltage is compared with the reference voltage Vref. If there is a voltage sag, then an error occurs. This error voltage is then sent to the PWM generator, which generates the firing, pulses to the switches of the VSI such that the required voltage is generated. The whole control strategy can be implemented in 2-ϕ rotating (d-q) coordinate system. To achieve the desired pulses, the firing pulses to PWM VSI are controlled. The actual bus voltage is compared to the reference value and the error is passed through a PI controller. The controller generates a signal which is given as an input to the PWM generator. The generator finally generates triggering pulses such that the voltage imbalance is corrected. The block diagram of the control circuit is shown in Figure. 5.

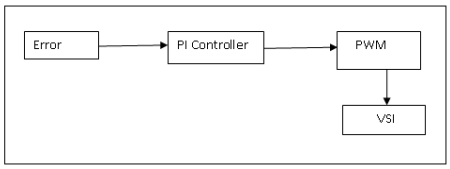

Figure 5: Control Circuit of DVR

Space Vector Modulation for Pulse Width Modulation Inverter

The Space Vector PWM (SVPWM) module inputs modulation index commands (U_Alpha and U_Beta) which are orthogonal signals (Alpha and Beta) as shown in Figure 6.

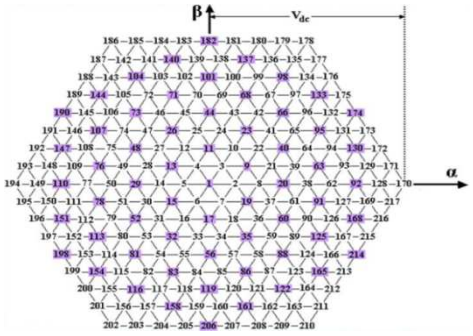

Figure 6: Space Vector Diagram for Nine-Level Switching

The Pulse Width modulation technique permits to obtain three phase system voltages, which can be applied to the controlled output. Space Vector Modulation (SVM) principle differs from other PWM processes in the fact that all three drive signals for the inverter will be created simultaneously. The implementation of SVM process in digital systems necessitates less operation time and also less program memory.

The SVM algorithm is based on the principle of the space vector u*, which describes all three output voltages ua, ub and uc.

$$u^* = 2/3.(ua + a.ub + a2.uc)$$

Proposed System Working Principle

DVR with Cascaded Nine-Level Inverter

In this section, DVR had been implemented with multilevel inverter of nine-level (A cascaded nine-level H-bridge inverter was designed). Three phase power supply is connected to the system. This proposed system's main goal is to

mitigate sag swell, THD and power factor correction. PCC voltage source purpose is maintained at constant voltage in distribution line. The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR. Though various topologies may be used to realize the VSC, multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Proposed circuit more preferred in high voltage and high power application. Multilevel converters can synthesize the output voltage with smaller steps and reduce harmonic content, while potentially resulting in smaller dv/dt thus lowering the electromagnetic effect. From Figure 9, nine- level inverter was designed with 3-arm H-bridge inverter by connecting in series to each other to make cascaded H-bridge nine-level inverter. The multilevel inverter was defined by (2N+1), here N is number of inverters connected in either in series or parallel. The output voltage of the nine-level inverter is the performance of the DVR with Cascaded H-bridge nine-level inverter is demonstrated for different supply voltage disturbances, such as voltage sag and swell. Harmonics are reduced by filters as shown in the figure. Figure 9shows 9 level cascaded H Bridge MLI by using unit vector of space vector modulation technique for PWM inverter. Figure 10. shows the simulation digram of unit vector this is a new control technique and the reference voltage estimated using the unit vectors digram.Unit vector means 16 values or angles entered in to the PWM generatorand in which place is reduced harmonics those values or duty cycle are considered. Without DVR, MLI THD is 19.84% and with DVR, MLI THD is 0.27% and without DVR, Power Factor is 0.78 and with DVR, power factor is 0.9993. From this data with nine level cascaded H inverter is more eficient or considered an excellent procedure for compensating the power quality problems

SIMULATION RESULTS

Simulation without DVR

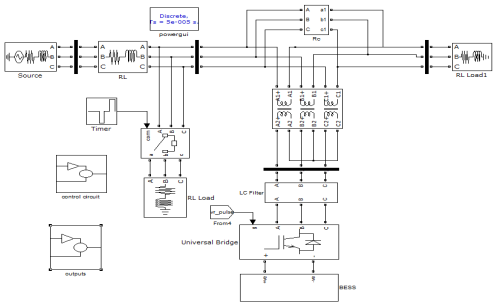

Figure 7: DVR without Cascaded Nine-Level Inverter

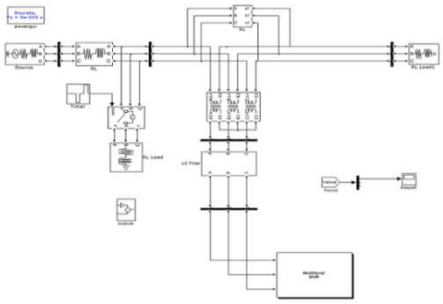

Figure 8: DVR with Cascaded H-Bridge Nine-Level Inverter

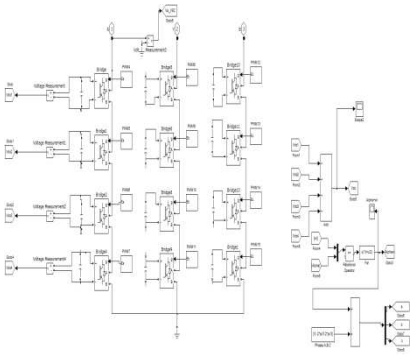

Figure 9: Simulation Design of Cascaded H-Bridge Nine-Level Inverter with SV Modulation for PWM Control Technique

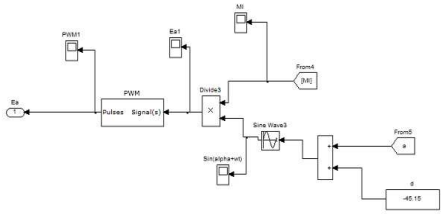

Figure 10: Simulation of Unit Vector(New Control Technique) (The Reference Voltage Estimated using the Unit Vectors)

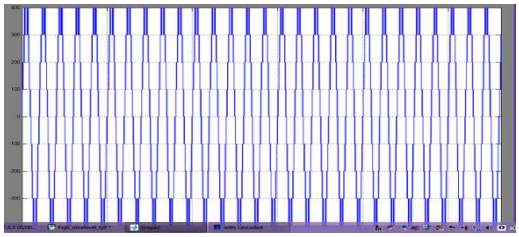

Figure 11: Injecting Voltage from DVR

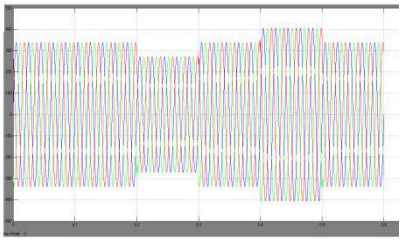

Figure 12: Sag and Swell at Source Side Voltage

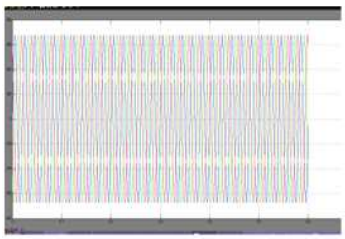

Figure 13: Load Voltage

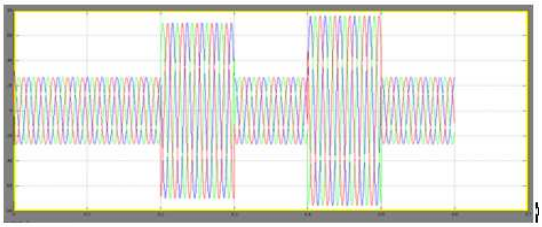

Figure 14: Output Voltage in VSC (Voltage of Cascaded H-Bridge Nine-Level Inverter)

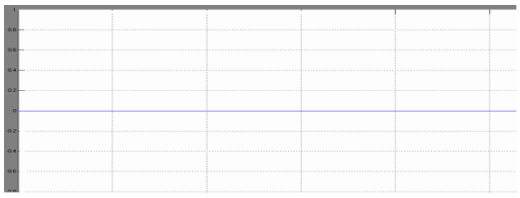

Figure 15: Reference Voltage (Vlref)

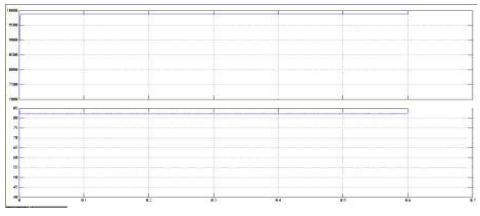

Figure 16: Voltage Magnitude at Load Side

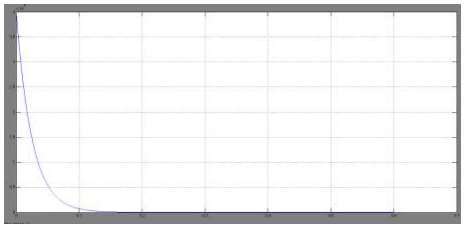

Figure 17: Vdc(dc Voltage)

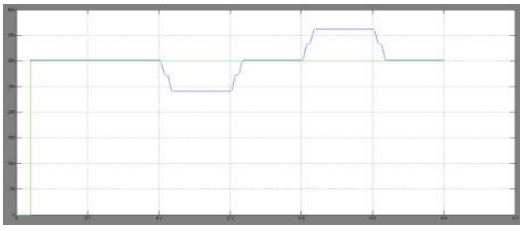

Figure 18: Voltage Magnitude at Load Side (Rms Voltage

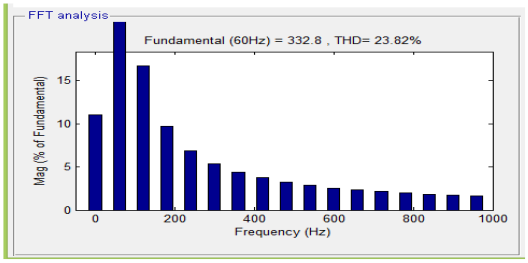

Figure 19: Harmonic Spectrum with ML

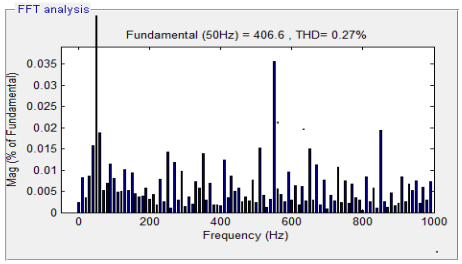

Figure 20: Harmonic Spectrum with MLI

Table 1

S.NO	TYP OF DVR	THD (%)
1	WITH OUT MLI	23.82
2	WITH MLI	0.27

Table 2

S.NO	TYP OF DVR	POWER FACTOR
1	WITH OUT DVR	0.78
2	WITH DVR	0.9993

CONCLUSIONS

To maintain balanced power quality problems in the distributed lines. This paper's scope is to mitigate the voltage sag swell, Total harmonics and Power factor correction. Power quality Circuit was developed by using Matlab/simulink software here used sim power system tool. The Synchronous reference frame theory has been used for estimating the reference DVR voltages. The control system implemented here is based on DQO technique which is a scaled error between supply side of the DVR and its set reference value. The references load voltage estimated using the method of unit vectors (trial or hit and error method), and the control of DVR has been achieved, with minimization of error of voltage injection. It is concluded that the voltage injection in phase with the PCC voltage results in minimum rating of DVR. The simulation results showed the DVR quality problems effectively and provided excellent voltage regulation.

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